# Intusoft Newsletter

intusoft *Personal Computer Circuit Design Tools*



## IsSpice For The Mac Weighs In

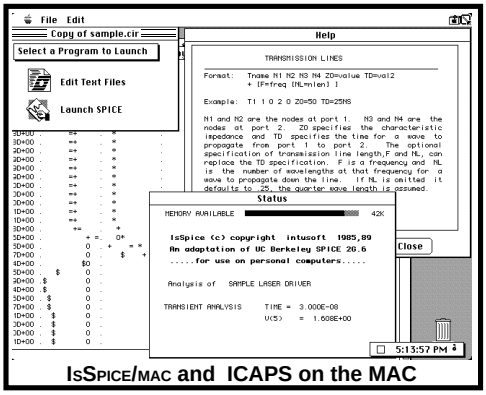
Intusoft has begun shipping IsSpice/mac, as well as the Spice preprocessing program, PreSpice/mac. Amazingly, IsSpice/mac can run on any Macintosh platform including the Plus, SE, SE/30, Mac II, IIx, and IIcx. IsSpice/mac is the only Spice simulator that can make this claim. Equally as important, the new Spice program can run with as little as 1 megabyte of RAM. These two features, along with the affordability, make IsSpice/mac the most versatile and powerful version of Spice for the Mac.

Both coprocessor (version 1.5M) and non-coprocessor (1.5MNC) versions are available. The coprocessor version can allocate RAM dynamically, therefore, circuit size is only limited by the amount of available RAM (1000 components per meg). The non-coprocessor version is limited to circuits of about 250 components in size (Maxmem=40K).

**In This Issue**



A unique feature of IsSpice/mac is the continuous display of the amount of available and used memory. This allows the user to decide if there is enough memory to complete a simulation without having to find out by exceeding the memory requirements. PreSpice/mac is also available and brings extensive model libraries and an easy to use menu drive interface to the Macintosh. See page 15-11 for benchmarks.




**IsSpice/mac and ICAPS on the MAC**

# Modeling Very High Speed Transimpedance Op-Amps

Over the past few years, a new operational amplifier (op-amp) technology has evolved. Using transimpedance techniques, it has become possible to break the slew rate limit of conventional op-amp technology. In this article we will develop the IsSpice model for this class of amplifier and discuss the design penalties incurred in realizing the higher speed.

## Conventional Op-amp Theory

Slew rate limit is the maximum rate of change in voltage that can be achieved for an arbitrarily high input overdrive. It turns out for a conventional bipolar op-amp, the topology shown in Figure 1, that the slew limit is closely related to gain bandwidth product. The following equations develop this theory:

1. $\left(\frac{dv}{dt}\right)_{max} = \frac{I_{EE}A_2}{2C}$
2. $\text{gain} = \frac{A_2}{ReC\,s} = 1 \qquad \text{when} \quad s = j2\pi\,Ft$

where Ft is defined as the gain bandwidth product. A2 and C are eliminated using equation 2.

3. $\left(\frac{dv}{dt}\right)_{max} = \pi\, I_{EE}\, Re\, Ft$

But Re is a function of current, according to the Ebers-Moll BJT model.

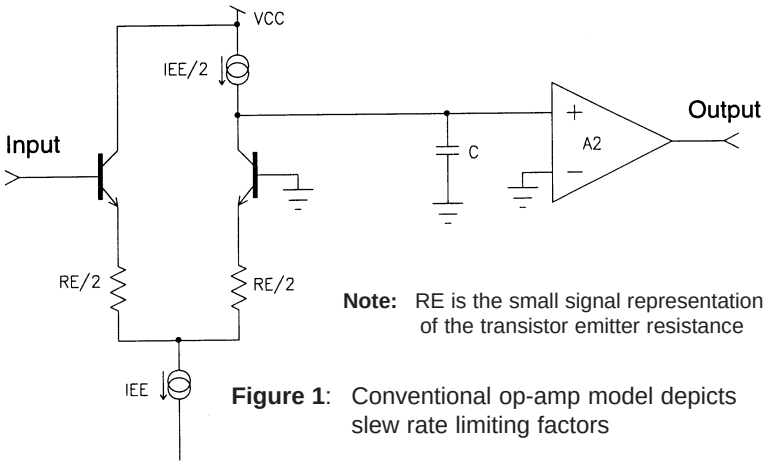
4. $I = I_S\left(e^{\frac{qV}{NkT}} + 1\right)$
5. $\frac{di}{dv} = \frac{q}{NkT}\left(I_S\left(e^{\frac{qV}{NkT}} + 1\right)\right) = \frac{q}{NkT} I$
6. $Re = \frac{NkT}{qI_{EE}}$

Therefore, substituting equation 6 into equation 3 yields:

7. $\left(\frac{dv}{dt}\right)_{max} = \pi\, N\, k\, T\, Ft / q$

**The symbols used in the above equations are:**

| | | | |
|---|---|---|---|
| k | Boltzmans constant | s | Laplace operator |
| T | Temperature in Deg. Kelvin | I | Current |
| q | Charge of an Electron | V | Voltage |
| $I_S$ | Junction Saturation Current | N | Emission Coefficient |




**Note:** RE is the small signal representation of the transistor emitter resistance

**Figure 1**: Conventional op-amp model depicts slew rate limiting factors

With this topology, only Ft can be adjusted to control the slew rate limit. This results in a full power gain bandwidth product that is considerably less than the small signal gain bandwidth product. Similar results are obtained for op-amps with FET front ends.

Changing the front end to use darlington transistors or adding external resistors for Re has only limited success in increasing the slew rate limit because these modifications also limit the useful common mode input range of the amplifier. If it were somehow possible to decrease the compensation capacitor value, then the slew rate limit could be increased. In order for this to happen, the loop gain must be reduced at Ft to maintain stability.

## The Transimpedance Topology

Introducing a slightly different topology can satisfy the stability criteria and reduce the size of the compensation capacitor. The block diagram shown in Figure 2 illustrates the central idea for achieving this result. If the input resistor, Ri, is less than the summing resistor, Rs; then the loop gain will be determined by the feedback resistor, Rf, and the input resistor, Ri. Changing from a differential to a complimentary topology will make even more dramatic improvements to the slew rate limit.

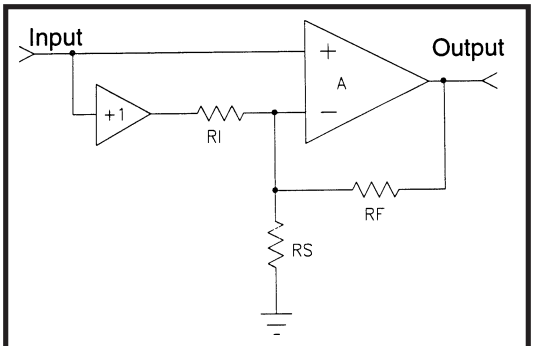



**Figure 2:** A Transimpedance op-amp topology

## Developing the Integrated Circuit Topology

The simplest front end for this kind of amplifier is shown in Figure 3. The slew rate for this circuit is very fast for positive inputs but slow for negative ones. The progression toward npn-pnp complementary symmetry shown

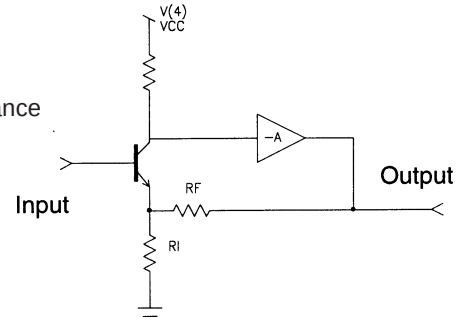
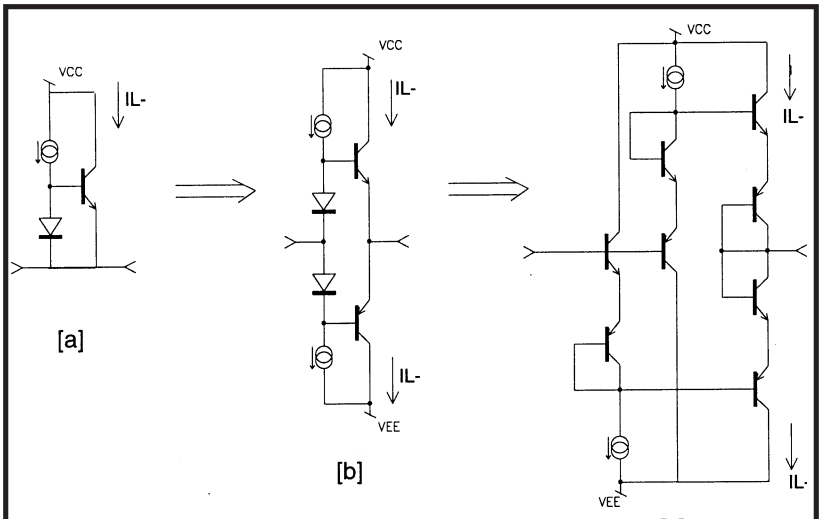



**Figure 3:** A Simple Transimpedance op-amp

in Figure 4 can be seen to give even greater slew rates. The current available to charge the compensation capacitor is limited by the input transistor characteristics and the bias current. Coupled with the factor of 5 given by a feedback attenuator, the slew rate is almost 2 orders of magnitude higher than for a conventional topology.




[a] A diode cancels the base emitter offset
[b] Complimentary symmetry cancels bias current
[c] P-N device offsets cancel in each complimentary half

**Figure 4:** A progression of front end improvements shows how offset and bias cancellation becomes progressively better

## Making an IsSPICE Model

Many IC design issues can be bypassed when developing a simulation model. What is needed for a valid simulation model is to duplicate the circuit performance seen at its pin connections; that is, the input, output, power, and compensation pins. Our circuit discussion, thus far, has been limited to the input stage. The output stage is sufficiently similar to conventional op-amps that we can borrow the output topology used in the PRESPICE generic bipolar opamp model. External compensation is used for Ft control and its implementation varies between vendors; therefore, performance at the compensation pin(s) is not included in the model. The model presented here can be modified to include this feature.

Besides modeling AC and DC performance, other features include input stage nonlinearities, input voltage and current offsets and bias, noise response, slew rate limiting, common mode gain, power supply rejection, output current limiting, reflection of load current to the power input, and output stage nonlinearities. The relation of output current to power supply current is also modeled. The complete model is shown in Figure 5. Figure 6 shows the performance of the model using parameters from a Comlinear CLC401 data sheet.

## How Model Parameters Affect Performance

In order to extend this model to other devices it is necessary to understand the relationship of model parameters to circuit performance. The major circuit parameters influenced by the input stage BJT model parameters are listed below:

| Model Parameter | Performance Parameter |
|---|---|
| RB | Eliminates right half plane zeros |
| VAF | Controls DC value for common mode rejection |
| I1,I2 | Controls input resistance, see Ri in Figure 2, and noninverting input resistance |
| CJC | Controls second order poles - phase margin and high frequency common mode rejection |
| KF | Enables 1/f noise modeling |

The difference between PNP and NPN parameters will produce some rise and fall time asymmetry. They will also control the bias current and offset voltage. Correlated parameters, such as temperature coefficients, will be more accurate if offsets are modeled in this manner.

## Model Parameters *(Cont'd)*

The remaining model parameters, shown in Figure 5, are described next:

The resistors; R1, R2 and capacitors C5, C6 model the current mirrors that connect the input stage to the IC interstage. They will scale with current (I1 and I2) and bandwidth. C1 controls the high frequency gain while G2 controls DC gain independent of high frequency gain. The output stage uses Beta and the I3 bias to control current limiting and quiescent output resistance. L1 and R5 model the output transistor gain bandwidth affects. C2, C3, and C4 account for device package capacitance.

## Adding Parameters

The most useful model is one in which data sheet parameters are included in the model. In this manner, variations in component performance can be analyzed and a range of component types can be substituted. Parameterized models also allow several op-amps to be simulated with a single generic model. Some of the parameters just fall out naturally; for example, input noise. Others are so closely grouped that the generic part usually doesn't need alteration; for example, output limits with respect to the power supply. There is a third group which, although important, is not mentioned in data sheets with sufficient frequency to be readily available. This last group is handled by the model itself; for example, differences in positive and negative slew limits or open loop transfer functions. You will find that these

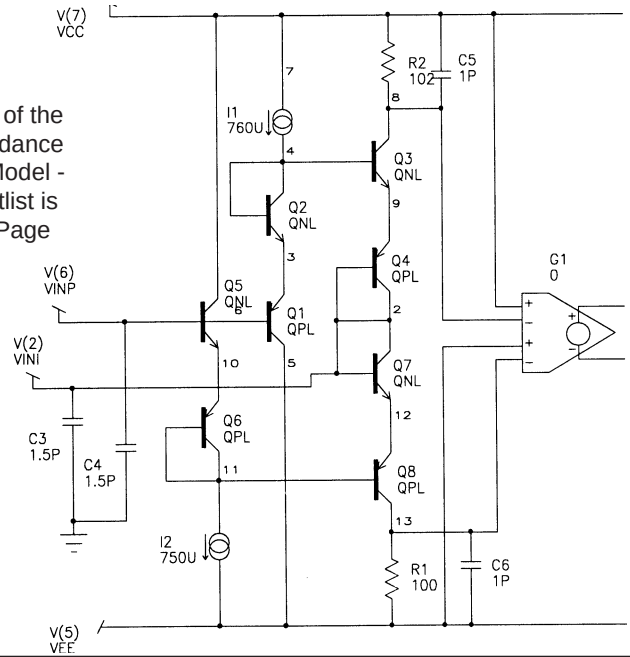



**Figure 5:** Schematic of the Transimpedance Amplifier Model - AMPC; Netlist is shown on Page 15-10.

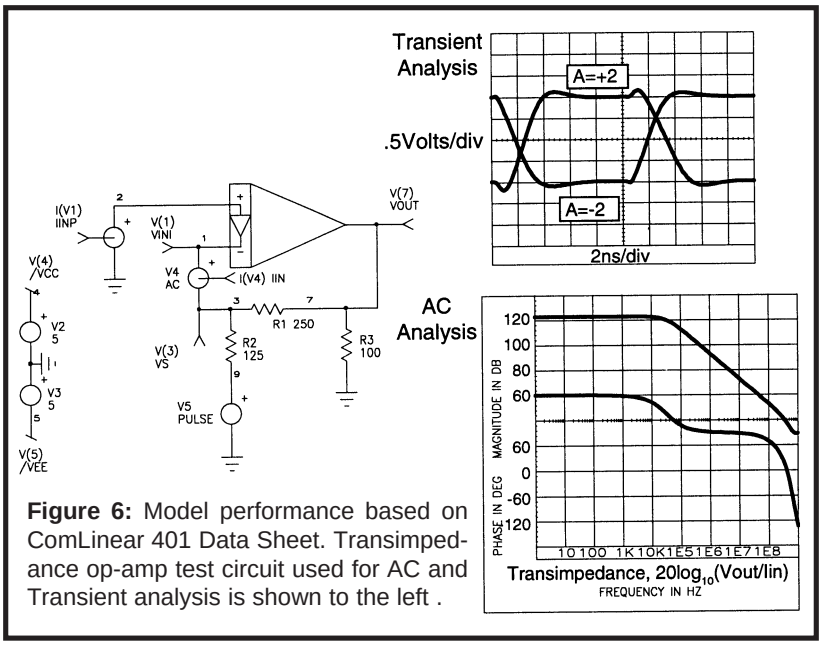
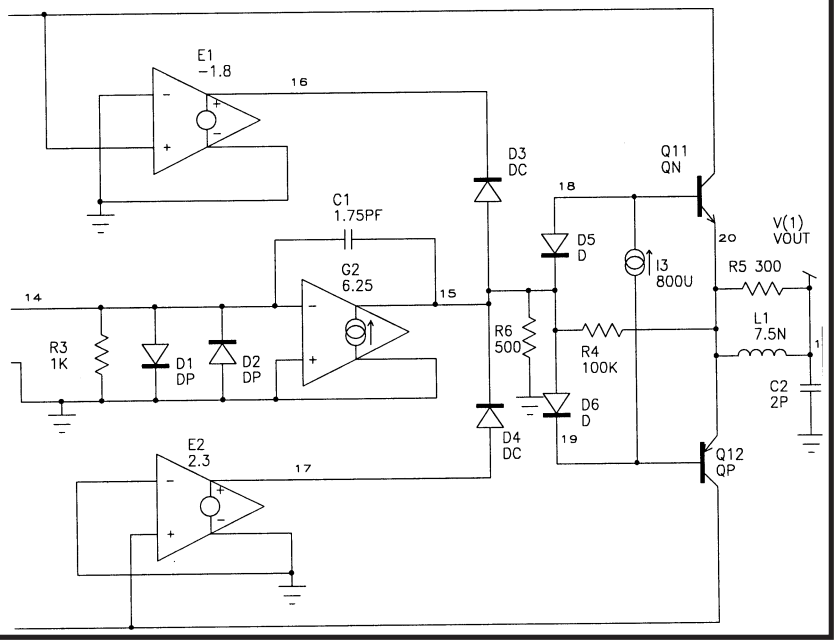



**Figure 6:** Model performance based on ComLinear 401 Data Sheet. Transimpedance op-amp test circuit used for AC and Transient analysis is shown to the left .

high frequency circuits are very sensitive to mechanical layout. Our book, SIMULATING WITH SPICE, the PRESPICE software package, and the July 1987 Newsletter all describe interconnect modeling techniques as well as modeling conventional bipolar/FET op-amps.



## Parameter List

The following parameters are used to describe the generic model:

| Name | Description | Typical Value | |
|---|---|---|---|
| **DVDT in V/sec** | Slew Rate Limit | 1200 V/Usec | [2] |
| **FC in Hz** | Bandwidth (-3dB point) | 150MEG | [2] |
| **RF in Ohms** | Feedback Resistor | 250 | [2] |

**Computed Parameters**

| Name | Description | Value | |
|---|---|---|---|
| RINI | Inverting Input Resistance | 400*FC/DVDT Ohms | [3] |
| RINP | Input Resistance | $10^4$RINI Ohms | [3] |
| GM | Transimpedance | $10^5$RINI | [3] |
| VOS | Input Offset Voltage | 75UV | [3] |
| IBIAS | Input Bias Current | 75NA | [3] |
| IBAISN | Inverting Input Bias Current | 10UA | [3] |

[2] Values must be consistent; that is, they must result from a single test.
[3] Approximate values that fall out of the model.

The following parameters have been compiled for several common op-amps. Other 5 and 15 Volt transimpedance op-amps may be modeled using similar data sheet parameters.

***15 Volt Model***

| | RF | DVDT | FC |
|---|---|---|---|
| **Analog Devices** | | | |
| AD9610 | 1.5K | 3500 | 100 |
| **Elantec** | | | |
| EL2020 | 820 | 500 | 50 |
| **Comlinear** | | | |
| CLC200 | 2K | 4000 | 95 |
| **PMI** | | | |
| OP260 | 5K | 200 | 8 |

***5 Volt Model***

| | RF | DVDT | FC |
|---|---|---|---|
| **Analog Devices** | | | |
| AD9611 | 1K | 1900 | 280 |
| **Comlinear** | | | |
| CLC400 | 250 | 700 | 200 |
| CLC500 | 250 | 800 | 150 |

To alter the generic model to represent the desired op-amp, just evaluate the expressions in the curly braces using the listed values. PreSpice users may perform list evaluation automatically by simply passing the parameters to the subcircuit using PARAM. The generic model shown is for a 5 Volt transimpedance op-amp. To convert the model to a 15 Volt op-amp representation just replace each instance of the number "1.2E-9" with "2.4E-9".

```
*****************
* PARAMATERIZED TRANSIMPEDANCE OPAMP,
*  FC, DVDT AND RF ARE THE PARAMETERS
.SUBCKT AMPC 2 6 1 7 5
*  - VIN 2, + VIN 6, OUTPUT 1
*  VCC 7, VEE 5
Q2 4 4 3 QNL
Q3 8 4 9 QNL
Q4 2 2 9 QPL
I1 7 4 {760U * (DVDT/1.2E9)^2 }
Q5 7 6 10 QNL
Q6 11 11 10 QPL
Q7 2 2 12 QNL
I2 11 5 {750U * (DVDT/1.2E9)^2 }
Q8 13 11 12 QPL
R1 13 5 {100 * (1.2E9/DVDT)^2  }
R2 8 7 {102 * (1.2E9/DVDT)^2  }
R3 14 0 1K
D1 14 0 DP
D2 0 14 DP
G2 0 15 0 14 6.25
C1 14 15 {2.2P * 250/RF * 150MEG / FC}
E1 16 0 7 0 -1.8 1
E2 17 0 5 0 2.3 1
D3 15 16 DC
* AMPC Netlist Continued
D4 17 15 DC
D5 18 15 D
D6 15 19 D
Q11 7 18 20 QN
Q12 5 19 20 QP
I3 19 18 800U
R4 15 20 100K
L1 20 1 {7.5N * 1.2E9/DVDT}
R5 20 1 300
C2 1 0 2P
R6 15 0 500
C3 2 0 1.5P
C4 6 0 1.5P
C5 7 8 {1P * 150MEG / FC}
C6 13 5 {1P * 150MEG / FC}
Q1 5 6 3 QPL
G1 14 0  POLY(2) 7 8 5 13 0 {5M *
+(DVDT / 1.2E9)^2}
+{5M * (DVDT / 1.2E9)^2}
.MODEL D D(CJO=1PF N=1.25)
.MODEL DP D(N=2)
.MODEL DC D(RS=.001)
.MODEL QN NPN(CJC=.5PF)
.MODEL QP PNP(CJC=.5PF)
.MODEL QNL NPN(BF=100 CJC={(.8P*150MEG)/FC } IS=1E-14 TF={.1N  * 150MEG/FC }
+ KF=3.2E-15  VAF=40  RB=35 )
.MODEL QPL PNP(BF=150 CJC={(1.2P*150MEG)/FC} IS=2E-14 TF={.15N  * 150MEG/FC }
+ KF=3.2E-15 VAF=40 RB=35 )
.ENDS
*******
```

## Transimpedance Op-amps; Made For Simulation

The transimpedance op-amp topology solves the problem of achieving power bandwidths on the order of small signal bandwidths. The penalty, however, is increased noise and front end bias sensitivity for low gain configurations.

The increased noise is due to the fact that the amplifier noise is amplified in accordance with the Rf/Ri ratio; a constant, while the signal gain goes as Rf/Rs. The equivalent input noise is then the product of amplifier noise and Rs/Ri, which is minimized as Rs approaches zero. On the other hand, the superb high frequency performance, high slew rates, and fast settling times offered by these monolithic structures is simply impossible with the older technology. So if you're working at high frequencies, need some gain in noise critical applications, or if noise is not a consideration, the transimpedance amplifier is a good choice.

Transimpedance op-amps are, however, very sensitive to printed circuit board parasitics and require a well thought out layout including good power supply bypassing and minimization of stray capacitances. These sensitivities preclude the use of a breadboard test environment. Viable test options include specialized test boards, final prototype test beds, or an IsSpice simulation; a somewhat more cost effective and expedient solution.

Our models presented here allow full nonlinear performance evaluation. The ability to simulate high frequency performance without breadboard parasitics will allow accurate prediction of production circuit performance.

## IsSpice Benchmarks

With the release of IsSpice/mac we thought that some comparative benchmarks would be of interest. Spice is an excellent indicator of a machine's performance because of the intensive memory references, coprocessor activity, and disk access. They can usually be more telling from a user standpoint than the common Linpack/Whetstone numbers. The benchmark circuits contain a mixture of AC, DC, and Transient analyses. The average index of performance was calculated by adding all the simulation times for the circuits listed below (except Long) plus 16 others, and normalizing to a 6 MegHz IBM AT. The Spice versions used were IsSpice/386 (v/386), IsSpice 1.41 (v/1.41), IsSpice/286 (v/286), and both new versions of IsSpice/mac (1.5M and 1.5MNC). Simulation performance for a MAC IIx was about 3-5% slower than for an SE/30. The benchmarks circuits used in the test are available at no charge by contacting Intusoft. Most of the circuits are from the file Bench.cir distributed with IsSpice.

### Technical Specifications and Memory Usage

| | | Nodes | Elements | Diode | BJT | Memory ! |
|---|---|---|---|---|---|---|
| 1 | DIFFPAIR | 14 | 12 | 0 | 4 | 10,608 |
| 2 | ECLGATE | 36 | 25 | 2 | 8 | 19,760 |
| 3 | OSC | 14 | 19 | 0 | 7 | 7,984 |
| 4 | 74LTTL | 27 | 16 | 3 | 5 | 15,296 |
| 5 | CHOKE | 4 | 8 | 2 | 0 | 9,776 |
| 6 | ASTABLE | 6 | 10 | 0 | 2 | 11,072 |
| 7 | SAMPLE | 14 | 15 | 1 | 3 | 14,400 |
| 8 | CHAIN | 28 | 12 | 0 | 10 * | 23,792 |
| 9 | EFIL | 54 | 118 | 21 | 15 | 68,016 |
| 10 | DIV4 | 107 | 256 | 60 | 30 ** | 84,920 |
| 11 | LONG | 1162 | 2967 | 622 | 305 ** | 1,025,808 |

* Indicates the number of MOSFETs used in the circuit
** Indicates the number of JFETs used in the circuit
! Memory is in bytes converted from the IsSpice .Options Acct Memuse value which is in 32 bit words.

### Benchmark Circuit Runtimes

| | 386/20 | 386/20 | AT/6 | AT/6 | Mac IIx | Plus | Vax 8700 * |
|---|---|---|---|---|---|---|---|
| 1 | 5.83 | 17.36 | 76.02 | 102.55 | 28.22 | 220.00 | 1.64 |
| 2 | 12.36 | 29.44 | 186.91 | 246.72 | 43.55 | 417.22 | 3.67 |
| 3 | .77 | 2.03 | 13.13 | 14.17 | 3.22 | 17.42 | .23 |
| 4 | 10.93 | 29.49 | 158.95 | 213.99 | 38.50 | 327.27 | 3.46 |
| 5 | 3.13 | 5.16 | 32.68 | 52.13 | 9.83 | 55.43 | .96 |
| 6 | 10.71 | 21.15 | 132.64 | 200.26 | 36.85 | 324.97 | 3.52 |
| 7 | 13.40 | 35.98 | 179.99 | 248.87 | 38.88 | 326.13 | 3.83 |
| 8 | 17.25 | 92.11 | 649.11 | 848.16 | 120.70 | 2179.50 | 4.93 |
| 9 | 40.75 | 124.85 | 660.23 | 1000.00 | 156.90 | 1247.90 | 12.21 |
| 10 | 141.00 | 376.56 | 2324.96 | 3011.46 | 555.30 | 6052.67 | 47.03 |
| 11 | 6549.00 | n/a | n/a | n/a | 24467.50 | n/a | 2311.35 |
| **Index** | **16.3** | **6.15** | **1** | **.75** | **4.25** | **0.40** | **50.9** |
| **NDP** | **387** | **387** | **287** | **287** | **68881** | **none** | |
| **Version** | **/386** | **/1.41** | **/1.41** | **/286** | **1.5M** | **1.5MNC** | **2G.6** |

* Vax times are CPU. Actual runtimes were 2X to 6X longer depending on the # or users.