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Personal Computer Circuit Design Tools

N E W S L E T T E R

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Back in 1986 we developed a little 17K Byte program to help us draw schematics for our manuals and newsletters. Many customer requests later, we are near the release date for a full SPICE schematic editor. The code has grown to over 170K

Bytes and is now in Beta site evaluation. With the variety of Schematic Editors available we went ahead with our own mainly because of the digital orientation of those products and the need to link presentation quality graphics with our simulator. We have added our own analog touch and have focused on a product for SPICE that can stand alone. Our feature article describes our new product and hopefully illustrates its ease of use. Even if you have existing schematic packages for developing production circuits you will find SPICE_NET just what you need for SPICE simulator input and output. As you flip through this newsletter you will find graphics generated using SPICE_NET coupled with Aldus PageMaker driving an Apple Laser Writer. Wouldn't you like your next IR&D or project report to look like this?

SPICE_NET Release Set for November

A new SPICE schematic entry program, SPICE_NET, will be released in November, see the inside back cover for ordering information. The program is used to create a complete SPICE input file from a schematic drawing. The schematic drawing is prepared using your IBM or compatible PC equipped with a graphics adapter and mouse. Resulting netlists are compatible with any SPICE simulator. Each SPICE component is represented with a symbol conforming to ANSI specifications. These symbols are given a special library that may be accessed by one or two key strokes. For example, a transistor is drawn on the screen by pressing "Q". When a number is entered first, an alternate representation, for example, a PNP transistors is drawn by pressing "2Q". The symbol

library can also be accessed using the pull down menus. Using both pull down menus and expert key commands makes the program fast to learn and lets the experienced user operate more efficiently.

There are 4 main menus shown below. Menus are accessed by either pointing using the mouse and pressing the left button or by pressing the function key indicated in the menu. A menu item is selected by either dragging the mouse and releasing the button, by using the keyboard arrows and the Enter key, or by pressing the key associated with the menu item. The key sequence to print the drawing to a file using HPGL syntax as shown would be "F1 P H".
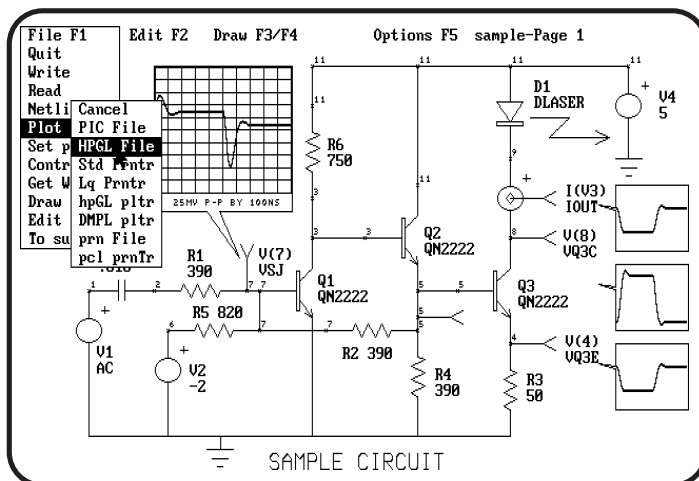

Figure 1. A screen dump from an EGA using an Epson LQ1000, reduced 50%, shows the IS-SPICE sample circuit.

Pull Down Menu Windows

SPICE_NET pull down menus work somewhat differently than Microsoft's Windows. When a menu is selected, you may move to "enabled" items or other menus. The mouse pointer will be automatically confined to the subject, unlike MS Windows, you must continue and make a choice. To do nothing, simply select "Cancel" or a window header. Some menus will scroll, for example, the subcircuit and symbol libraries. If a single command is executed, the the menu will automatically "roll up", otherwise it remains down for you to select additional items.

Making a Drawing

Schematic Drawings are made by placing parts on the screen and moving them around. The interconnection happens automatically. When parts don't fit together, a special part, called a wire, is used to make the connection. Wires are special because they will connect to all pins they cross and any part pin can be connected anywhere along a wire. Wires only lie in the horizontal or vertical plane, an automatic right angle is made when you move diagonally.

To move a part, place the mouse on the part and press the left button. When a bounding box appears, drag the part around and release the button when its positioned properly. To move a group of parts, place the mouse at one corner, press the left button and quickly move toward the opposite corner. A box appears in which all enclosed parts are selected upon release of the button. The parts are erased and replaced by a bounding box which can be moved to a new position.

Adding Labels

Text can be added in three ways. First, as shown in Figure 2, the part value and reference designation can be placed on the drawing. This informations can be placed in either a one line (Wide) or two line (Tall) format. Second, a label can be added to waveforms as shown at test point Y4 in Figure 2. Third, a line of text can be placed anywhere on the drawing. It can be added to a part or it can stand by itself.
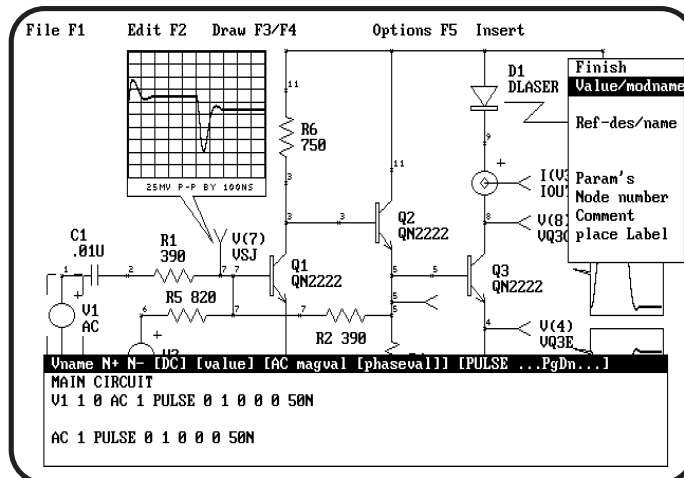

Figure 2. A second EGA Screen Dump shows the how the Label menu adds to or changes the attributes of a part.
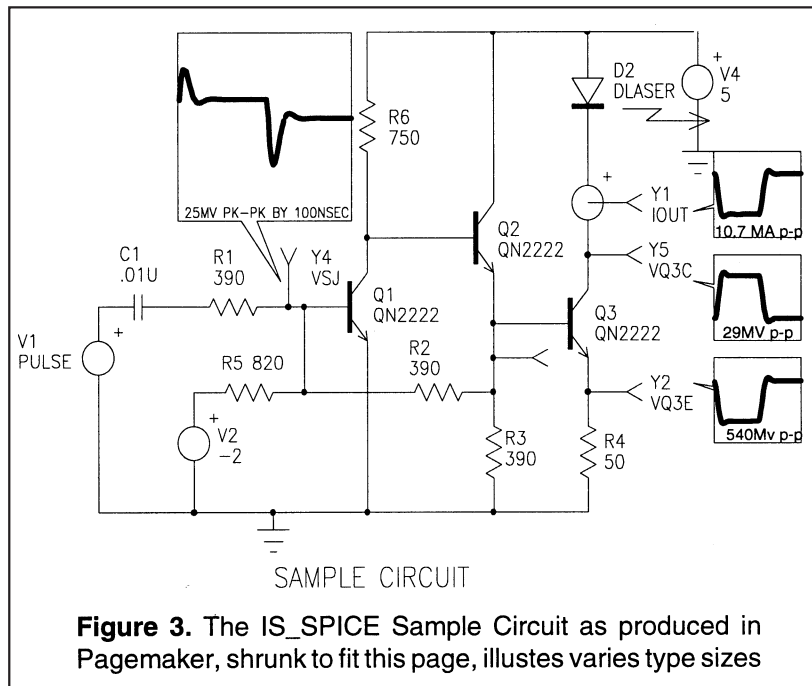
Each text entry can be selected to be one of three type sizes; 8, 12 or 18 Point. Only text added by the third method can be rotated or flipped. Text that is rotated will always read right side up, left to right if it is horizontal. Vertical text can run up or down.

Adding Values

Figure 2 shows the menu that is used to add or change values and place labels. Reference designations and node numbers are selected automatically by the program. You can override these choices and add part specific information. Each SPICE part has a syntax summary displayed automatically. The menu can be accessed either through F2 Label or by pressing the Tab or Backspace key. Tab will move forward through the part list and Backspace will move backward, making it easy to add values after drawing the schematic.

Output

Schematic Drawings can be made on a variety of devices. SPICE_NET will automatically interface with HPGL plotters, Epson or Epson LQ dot matrix printers. A "PIC" file format can be used to move the schematic drawing to Microsoft Windows applications such as Micrografix !Draw or

Figure 3. The IS_SPICE Sample Circuit as produced in Pagemaker, shrunk to fit this page, illustes varies type sizes

Aldus PageMaker. Figure 3 shows how the sample circuits looks in this form compared to the screen views in previous figures. The drawings in this newsletter, except for those LQ screen dumps, were produced using PageMaker and an Apple LaserWriter plus Laser Printer. Once in PageMaker, the netlist features are no longer needed so that changing the size and aspect ratios and adding different print become possible.

Displaying Waveforms

Unique to SPICE_NET is the ability to bring waveforms in from Intu_Scope. A special subcircuit library entry called a Frame is used to contain a waveform. The Get WFM menu under the main File menu presents the information you need to make a selection as shown in Figure 4. When waveforms are drawn, they are brought in from the latest analysis to keep your information current.
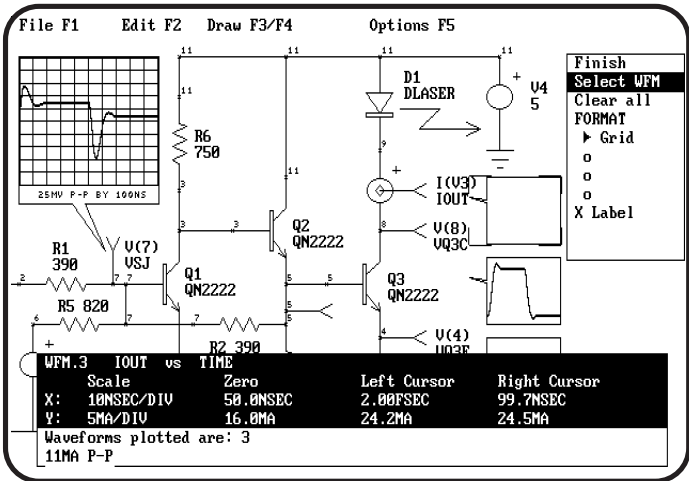

Figure 4. This Screen Dump shows the how the Intu_Scope waveforms are selected

Subcircuits

A subcircuit library containing symbolic representations of all subcircuits in the PRE_SPICE library is stored in a special directory. Pin connections are used to automatically create the node list. Parameter names are given where applicable for calling circuits using the PRE_SPICE extended syntax.

Zoom, Grid Snap and Pin Snap

There are 6 zoom levels ranging from 1/2 size to 16 times magnification. To change the view size, point to the new screen center and select the zoom level, or choose Fit Screen to get your whole drawing into the highest magnification level.

Grid snap is used to make it easier to draw straight lines and make different symbols interconnect. It is variable from .001 inches to .25 inches and defaults to .1 inch. Pin Snap is a similar concept that aids netlist connectivity. It is selected automatically and is about .25 inches as measured on your screen, so that its absolute value varies with zoom magnification. When a symbol pin is within the pin snap distance of another pin, the entire symbol will be dragged to the nearest pin when the mouse button is released, otherwise the starting point of the symbol will snap to the nearest grid point.

Making Symbols

A built in Symbol Editor allows you to make new symbols. Symbols can be made from an old symbol, a collection of old symbols and from basic objects. Basic objects are lines, arcs, filled rectangles, circles, text and pins. Pins are added in the order required by SPICE, or not at all for artwork. Symbols can be stored in a built in SPICE part library or in a Subcircuit library file. The program comes with all the symbols needed to build circuits from SPICE parts and PRE_SPICE library elements.

The SPICE Net List

Spice netlists are created automatically as the drawing progresses. Nodes and values that have not been assigned are displayed as xx. When the drawing is fully interconnected, the nodes and part reference designations will have been made. You must then enter the label menu to insert values, model names, other SPICE parameters and comments. The test point is a special component that causes a .PRINT statement to be incorporated. The label menu for test points is special. You may turn the AC, DC and Transient analysis controls ON or OFF and you may give the test point an alias name. The alias will be printed on the label and a *ALIAS line will be added that will be used in a later version of Intu_Scope to identify certain nodes. This feature is necessary so that schematic revisions that change node numbers will still refer to the same test point. It also overcomes the Intu_Scope limitation on character

length for a .PRINT argument. To complete the SPICE netlist, you must enter the File-Control menu to identify the type of analysis or insert special directives such as those required for the Optimizer or Monte Carlo Analysis. This menu displays three lines at a time with the center line reserved for editing. A contest sensitive syntax summary is displayed at the same time. Subcircuit library references are found here, they are added automatically when a subcircuit is called and you may edit them, for example, LIN.LIB could replace NONLIN.LIB to get a simpler model level for an op-amp.

Putting it all together, you get the complete netlist on program exit or by asking for it in the File menu. You can also view and edit the entire netlist with the PRE_SPICE screen editor by selecting Edit Net in the File menu. The Netlist portion above the *SPICE_NET comment line will not be changed once the netlist is created. You can use this area for special circuits or control statements. The netlist shown below was created for the sample circuit shown in previous figures.

Table 1: SPICE_NET Listing for SAMPLE.CIR

```
SAMPLE
.OPTIONS ACCT                              R2 3 4 390
*SPICE_NET                                 R3 4 0 390
.TRAN 1N 100N                              R4 5 0 50
*INCLUDE C:\SPICE\CIRCUITS\DEVICE.LIB      R5 7 3 820
.MODEL D1 DLASER(N=2)                      V2 7 0 -2
*ALIAS  I(V3)=IOUT                         V3 8 6
*ALIAS  V(3)=VSJ                           V4 9 0 5
*ALIAS  V(5)=VQ3E                          R6 9 10 750
*ALIAS  V(6)=VQ3C                          Q1  10 3 0 QN2222
.PRINT TRAN  I(V3) V(5)  V(4)  V(3)        Q2  9 10 4 QN2222
.PRINT TRAN  V(6)                          Q3  6 4 5 QN2222
C1 1 2 .01U                                D2 9 8 DLASER
R1 2 3 390                                 V1 1 0 PULSE 0 .5 0 0 0 50N
                                           .END
```

Shown to the right is a portion of a UA741 op-amp schematic that illustrates various component rotation and mirror image capabilities. Also shown is the capability to connect transistor base leads with co-linear wires and maintain proper "dot" notation to indicate connectivity. Notice the power of transporting the drawing file to PageMaker so that it can be cropped and edited into the text.
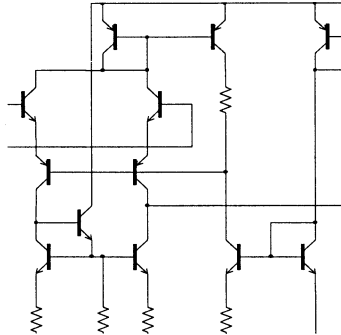
Optimizer Applications

Since releasing the PRE_SPICE version 2.0 update at the end of April we have found some interesting applications for the Optimizer. There are many cases where steady state solutions are needed for nonlinear transient simulation problems. In the past, this has meant running a transient simulation for a long time, perhaps thousands of switching cycles. It turns out that the optimizer can be used to provide feedback for the simulation which makes these impractical simulations feasible.

The trick is to make an objective function, using Intu_Scope, that is uniquely maximum at steady state. Second, it is necessary to identify a simulation input parameter, such as a capacitor initial voltage, that must be computed to establish the steady state condition. If there is more than a single state variable that must be found, then there must exist an algebraic relation between them that can be computed using the parameter passing program, PARAM.EXE.

Here's how it works for a 60Hz transformer-rectifier circuit with a capacitive load, the circuit is shown if figure 6. The circuit is at steady state when the output voltage at the end of one cycle is the same as at the beginning of the simulation. To turn this into a function that is maximum at steady state, one uses Intu_Scope to measure and square the average value and take the reciprocal of the result.

Objective function = $1 / (V_{initial} - V_{1cycle})^2$

Figure 6. Optimizer finds the steady state solution
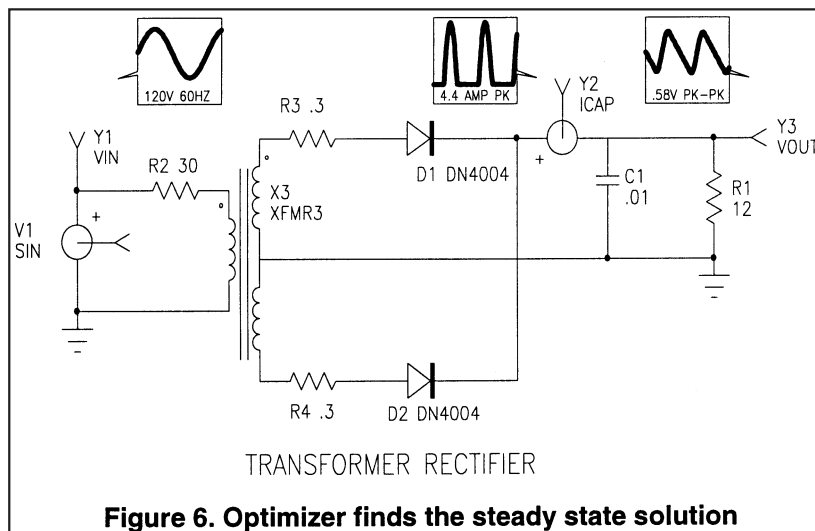
The objective function is then maximized by adjusting the load capacitor initial voltage. The maximization is performed by the optimizer program which makes repeated simulations using IS_SPICE and objective function measurements using Intu_Scope. The measurements then guide the program in its selection for the next capacitor initial condition in a manner that converges toward the objective function maximum. The optimizer control statements needed to find the steady state condition are shown in the following PRE_SPICE source listing.

```
TRANSFORMER RECTIFIER
*INCLUDE XFMR.LIB
*SPICE_NET
.TRAN 100U 20M
*INCLUDE C:\SPICE\CIRCUITS\DEVICE.LIB
I1 0 5 PULSE ILOAD 0
*OPT ILOAD=.8 TO 1.2
*ALIAS  V(6)=VQ1
*ALIAS  I(V)=IQ1
*ALIAS  V(5)=VOUT

.PRINT TRAN  V(5)  I(V) V(1)  I(V1)
D1 6 4 DN4004 IC=-12
D2  8 4 DN4004 IC=-12
C1 5 0 .01
R1 5 0 12
V 4 5
R2 1 2 30
R3 3 6 .3
R4 9 8 .3
X3 2 0 3 0 9 XFMR3  {RATIO=.1 }
V1 1 0 SIN 0 170 60
.END
```

We have also performed similar operations for a switching regulators in discontinuous conduction. The case shown in figure 7 was used to find steady state conditions for a fixed duty cycle. We also discovered that duty cycle could be adjusted to cause a specified output if steady state was defined to occur when the integral of difference between the desired output and the measured output was zero. Squaring and taking the reciprocal of this measurement made a unimodal function that was maximum at steady state.

Initializing without UIC

As an interesting aside, we found that circuit initialization was a problem for the IRF150 subcircuit. When UIC is used with the transient analysis, you must correctly specify all initial conditions to avoid a start up transient. To get around this problem without rewriting the subcircuit definition, we initialized the output with a pulse current source that turned off at the beginning of the simulation. The UIC directive was not used, instead the program automatically computed all the correct initial conditions and there was no start up transient.

Coupled inductors need non zero initial currents

If you make transformers with coupled inductors you will frequently get a real indefinite error when running IS_SPICE because of numerical underflow. To prevent this you must give the inductors a small non zero initial condition. Alternatively, use the PRE_SPICE transformer model.

Figure 7. Steady state solution for a DC-DC Converter in Discontinuous Conduction
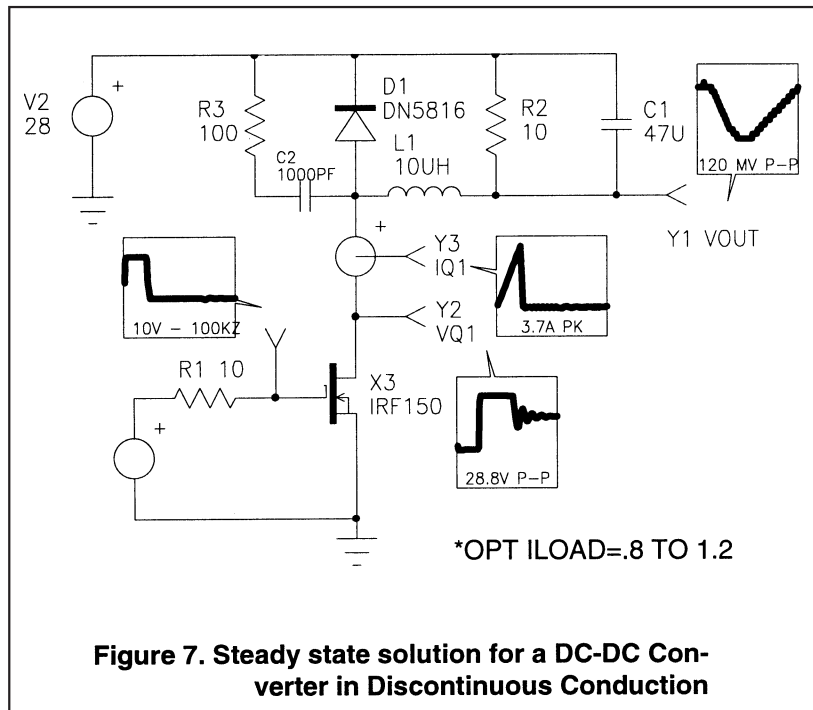
The optimizer works by adjusting a simulation input parameter to maximize a resultant measurement. The measurement, called the objective function, is made using Intu_Scope. The optimizer then computes its estimate of the control parameter for the next simulation. For this circuit we chose to control the initial load current. The optimizer then made the final voltage equal to the initial voltage by maximizing $1 / (Vfinal - Vinitial)^2$. The steady state results are shown.