The two buck regulators on the Microchip PICtail Daughter Buck/Boost boards were programmed using 2 control algorithms. First, a Modified Proportional Integral Derivative, MPID, algorithm was coded. This algorithm cancels the poles and zeros of the power filter. The modification consists of adding a lag to compensate for the zero caused by the filter capacitor ESR. Without this cancellation, the bandwidth can be severely limited because there would be no high frequency roll-off. Ideally, this approach can achieve deadbeat response to a commanded reference step. Unfortunately, power supplies are not required to respond rapidly to changes in reference voltage. Instead, they need to reject changes in input voltage and provide a stiff response to load current changes. The deadbeat issue is further complicated by the computational delay and nonlinear behavior of the filter inductor and filter capacitor. The step load response shown in Figures 3 and 4 illustrates ringing of the output at t he L-C filter resonant frequency. The amplitude of the voltage response is attenuated when the controller bandwidth exceeds the L-C resonant frequency. Limiting the error signal limits the rate at which the error can be corrected, thus implying a startup current limit of C*Vlimit/Tsample. This limit also reduces voltage overshoot so that no special slow

start algorithm is needed. Over current protection can't be achieved using the MPID method without sensing either load or inductor current. The second method uses Virtual Current control to make an inner control loop proportional to inductor current. Notice that the derivative term in the MPID method senses change in voltage across the filter capacitor. But the Virtual Current feedback is proportional to the integral of voltage across the inductor, a much less noise prone procedure. Virtual inductor current is found by simulating a "Plant Model" and extracting inductor current as a hidden variable. This method is more costly in terms of DSP resources, but it eliminates any need to measure load or inductor current. The plant model works by introducing another control loop that matches the plant output voltage with the measured output voltage. The resulting error is driven to zero by controlling the plant load current. This Virtual Current is then used to make an inner current mode loop and also enables current limiting to protect against overloads, including short-circuited output. The current control algorithm also works when the load supplies power and the buck converter operates in a boost mode. Buck-Boost symmetry occurs when the PWM switch has FET's in both legs.

3 result

Start-up Buck2

output voltage

1.00m

200u 600u

time in seconds

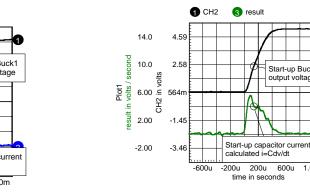


Figure 2, Virtual Current Control Startup Test Results

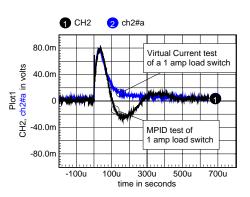


Figure 4, Load Switching Test Result

1 CH2 2 result 5.00 14.0 Start-up Buck1 3.00 output voltage 10.0 Plot1 CH2 in volts 1.00 6.00 -1.00 2.00 Start-up capacitor current -3.00 -2.00 calculated i=Cdv/dt -200u 200u 600u 1.00m -600u time in seconds

Figure 1, MPID Startup Test Results

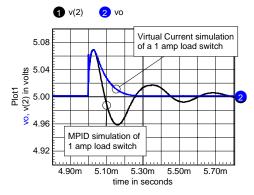


Figure 3, Load switching simulation results