Control Systems Sidebar Much of the literature concerning digital control of SMPS uses a proportional-integral-differential (PID) controller, sensing only the output voltage. The “optimum” control transfer function is the reciprocal of the L-C filter gain followed by a digital integrator. This gives the so-called deadbeat response by making the open loop transfer function

$$A=z^{-1}/(1-z^{-1})$$

which results in a closed loop transfer function of $G=z^{-1}$ (substitute A into G=A/(1+A)) so that the output reaches the input in one sample period. The error to a step input will be exactly zero at the next sample time. This concept is borrowed from motor control systems, which has the objective of rapidly tracking a position control signal. Figure PID shows how the controller responds to the control voltage command and the load step.

The SMPS control problem is different because the reference doesn’t change except at startup. The desired response characteristic is zero output impedance and a null input to output transfer function. Moreover, the noise produced by the switching action must be filtered at the input in order to eliminate interference with other circuits. Complicating matters even more, the output filter capacitors loss (real part) stays at a constant fraction of its impedance, making the high frequency ESR and the resonant damping resistance different. These additions make the system far more complex; perfect pole-zero cancellation is not practical.

The biggest problem achieving optimum PID controller response is the ill-behaved filter capacitor; its ESR adds a zero, preventing high frequency roll-off. Moreover, the ESR is not constant over frequency; it increases at lower frequencies. Modifying the PID control by inserting a pole to continue the roll-off (matching the undesired zero) mitigates the control problem. PID compensation eliminates the L-C filter resonance by pole-zero matching. It is necessary to consider the effect of component tolerances on stability margins. A general rule of thumb is to force the complex zeros to occur at a frequency slightly below the L-C pole frequency. By doing that, the frequency response consists of a lead-lag, approaching 180 digress at resonance which gives increased phase margin. On the other hand, if the compensating zeros occur at a higher frequency than the L-C poles, a phase lag-lead occurs, destabilizing the system at low gains. Gain reduction is a naturally occurring situation for large signals because of controller saturation (Duty ratio is limited between 0 and 1). Therefore a lag-lead characteristic makes it possible to enter large signal instability at start-up. Then the nominal offset in matching needed to guarantee stability results in increased ringing at the L-C resonant frequency for the nominal case.

Interestingly, the L-C characteristic impedance, sqrt(L/C), is proportional to sqrt(1/Fs) so that the damping of the resonance will go down with increased switching frequency. The reduction in impedance comes about because the filter inductor is made smaller to accommodate the same switched ripple current. Size and cost of the inductor are also reduced, so that the switching frequency should be increased until the stray inductance causes output noise to increase or because switching losses cause unacceptable degradation in performance. For the problem considered here, switching at 300kHz is about optimum.

An alternative controller uses peak or average current detection to turn off the PWM. This is the most often-used compensation

scheme for an SMPS. It is really a dual loop controller, with the inner loop proportional to inductor current. The outer loop is usually an integrator with a lead-lag stabilization network (nearly PI compensation). Overshoot tends to be eliminated if the phase margin is above about 60 degrees. The inner loop is similar to the derivative feedback, but it also contains a DC component equal to the load current. This inner loop reduces the control system from a lightly damped second order system to a first order system, with a pole at the L-C resonant frequency. This eliminates the pole-zero matching problem, making the current controller more robust with respect to component tolerances. The analog version is faster than a similar digital version because of the DSP computational delay. That slightly reduces the inner loop bandwidth, making the overall control bandwidth a bit lower than can be achieved with a modified PID controller.

The current controller gives better audio susceptibility results , namely minimizing vout/vin gain. The modified PID controller contains more switching noise at the duty ratio control point. In either case, noise levels are within acceptable limits, mostly affecting the A/D converter in a digital system and op-amp slew rates in analog systems.

The current loop requires measurement or estimation of the average inductor current. Using a plant model proposed here, the average current in the inductor can be recovered and combined with the estimated ripple current to form the predicted peak current. Refer to figure 1 and figure 3 to see how the peak current is used and how it's reconstructed based on observed and hidden states. The penalty for DSP current mode control is an increase in computational delay. Over time the penalty will become vanishingly small because of Moore's law. Circuits and waveforms that form the basis of this discussion can be found down loaded from

www.intusoft.com/DSP/PID.zip

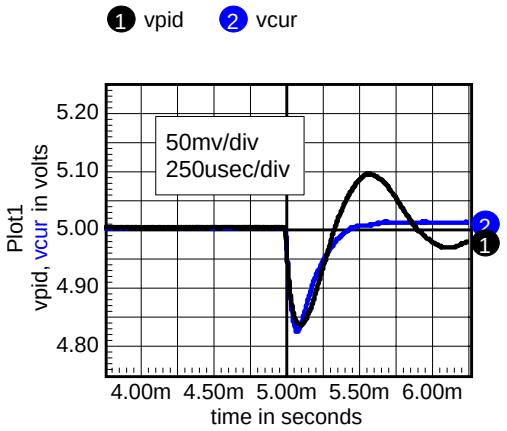

Figure PID, Test results show the PID waveform ringing at the L-C resonant frequency, but increased switching frequency mitigates the affect.

.